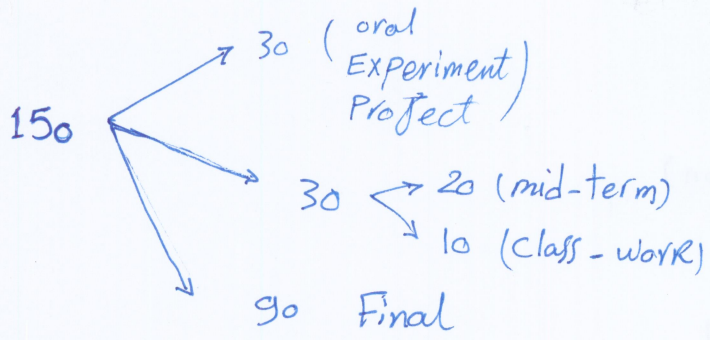
Digital Lec (1)

27/9/2016



* Course Contents :

- Logic families and its characteristics.
- EnCoder / Decoder
  Multiplexer / Demultiplexer } Combinational logic circuits
- Sequential logic circuit ⇒ flipflop
- Counters
- Shift Registers

* Types of logic families : (Based on its Basic elements)

- TTL (transistor - Transistor Logic)
  - Basic element BJT (0 ⟶ 5 V)
- ECL (Emitter coupled Logic)
  - Basic element BJT (negative Power-supply)
- CMOS (Complementary MOS (Metal-oxide-semiconductor))
  - Basic element ⇒ Both PMOS, NMOS

* Integrated circuits (ICs)

- SSI (Small Scale Integration)
  12 gate / chip

- MSI (medium Scale Integration)
  12 ~ 99 gate / chip

- LSI (large Scale Integration)
  1000 gate / chip

- VLSI (very-large scale Interation)
  100,000 gate / chip

⇒ More development chips ⟹ faster, cheaper

⇒ 7400 , NAND , 4 gate / chip

* Subfamily TTL

* Low Power
* Fast TTL
* Advanced TTL As TTL
* ALs TTL
  (Advanced Low Power schotIKy)

SN 74 ALS XXX A

TTL — family type

(74) → Ic Max temp.
0 → 70°

74f → TTL
74Cf → CMOS

(54) → TTL used for → military applications
(max temp. 55° → 125°)

(SN) → manfcature الشركة المنتجة

- SN → Texas instrument
- S → signetics
- DM → national instrument

(A) → اخر رمز

(Package نوع)

سيراميك — بلاستيك

N → Plastic - dual - in - line

W → ceramic Package

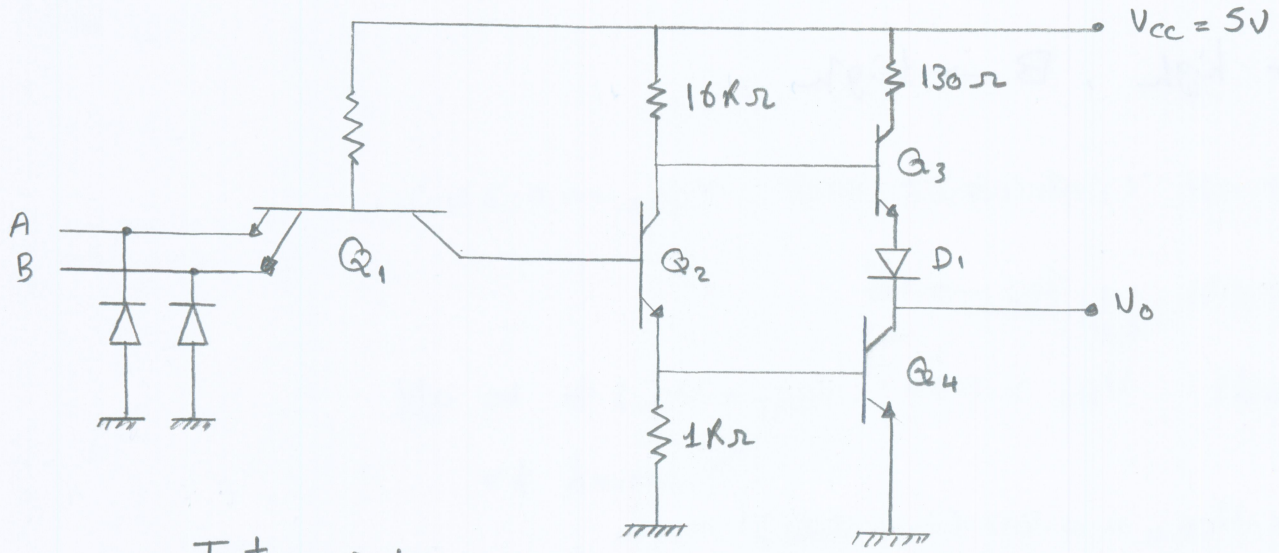
(XXX) → IC رقم الـ

138

Gate وتعبر عن نوع الـ

* 7400 (NAND Gate)

fundamental (Basic) TTL



Totem-pole NAND gate

Q_1 → Multi-emitter transistor

Q_3, Q_4 → totem pole transistors

Q_2 → control of Q_3 & Q_4

(*) $A = 0$ $B = 0$

$Q_1 \rightarrow$ ON (Saturation stat) $\rightarrow$ $V_{CE_1} = 0.2\ V$

$Q_2 \rightarrow$ off

current flow through Q_3 to V_{out}

$Q_3 \rightarrow$ ON

$Q_4 \rightarrow$ off (No Base current)

* $V_o = V_{cc} - V_R - V_{Sat} - V_{D_1} = V_{cc} - I*(130\Omega) - V_{D_1} - V_{CE_{sat}}$

$\cong$ 3.4 V (Logic high)

(*) A $\rightarrow$ high , B $\rightarrow$ low
or
A $\rightarrow$ Low , B $\rightarrow$ high
} Same analysis as the previous stat

- Note : D_2 , D_3 $\Rightarrow$ protection from high negative voltage

(*) A $\rightarrow$ high , B $\rightarrow$ high

$Q_2 \rightarrow$ ON (saturation stat $V_{CE_2} \rightarrow 0.2\ V$)

$Q_4 \rightarrow$ ON , $Q_3 \rightarrow$ off

- Q_3 needs $V_{B_3} > 1.4V$ ($V_{BE_3} + V_{D_1}$) to be ON
(V_{BE_3} around 1 V)

* $V_o = V_{CE_4} = 0.2V$ (low state)

note :

$D_1 \rightarrow$ Makes only one of "Q_3 , Q_4" $\rightarrow$ ON while the other one $\rightarrow$ off